# Rajanya Shrivastava

Junior Electrical and Electronics Engineering Rajiv Gandhi Institute of Petroleum Technology, Jais, Amethi

# EDUCATION

| Degree/Certificate | Institute/Board                     | CGPA/Percentage | Year |
|--------------------|-------------------------------------|-----------------|------|
| B.Tech., EE        | Rajiv Gandhi Institute of Petroleum | 8.63 (till 4th  | 2026 |
|                    | Technology, Jais, Amethi            | Sem)            |      |
| Senior Secondary   | Chapra Central School, Chapra/CBSE/ | 93.8            | 2021 |
| Secondary          | Chapra Central School, Chapra/CBSE  | 93.8            | 2019 |

# **PROJECTS** (ONGOING)

#### 3-tier VLC Network Data Rate Optimisation

- Supervisor: Dr. Shivanshu Shrivastava
- Utilized machine learning techniques to optimize data rate in a 3-tier VLC network.
- Developed a model that predicts the maximum data rate achievable under varying network conditions.
- Analyzed network performance across multiple tiers to identify key factors influencing data rate.
- Achieved significant improvement in data rate by fine-tuning parameters using the ML model.

# VLC Networks and Energy Harvesting

Supervisor: Dr. Shivanshu Shrivastava

- Integrated a 3-tier network model with energy harvesting mechanisms to enhance overall system efficiency.
- Investigated energy harvesting techniques to power network nodes and reduce dependency on external power sources.
- Applied machine learning algorithms to predict optimal energy harvesting configurations and minimize latency in network operations.
- Showcased potential use cases for sustainable network operations by leveraging harvested energy in resource-constrained environments.

# SCHOLASTIC ACHIEVEMENTS

- Top Ranker: From LKG to 12th
- Top 5 Ranker: B.Tech, EE (Till 4th Semester)
- National Level Finalist: Represented Bihar in 25th NCSC, Ahmedabad
- Gold Medalist: SOF Olympiads
- Finalist: Dark Patterns Buster Hackathon-2023, IIT-BHU

#### SKILLS

- Hardware Description Languages: Verilog, System Verilog
- Software programming Languages: Python, C, MATLAB
- Tools: ngSpice

# **POSITIONS OF RESPONSIBILITY**

- General Secretary, IEEE RGIPT SB
- 11th Class Coordinator, Gyanarpan A joint initiative of HAL and RGIPT
- Designing Head, E-cell, RGIPT

# EXTRA-CURRICULAR ACTIVITIES

- Hosted workshop on "Intellectual Property Rights" sponsored by Council of Science and Technology, UP
- Hosted Departmental Orientation for session 2023-2024 and 2024-2025
- Hosted the inagural session of SERB Sponsored Five Days Karyashala on Artificial Intelligence and Internet of Everything
- Aug, 2024 till date March 2024 - till date Aug, 2023 - Aug, 2024

April 2024 - till date

September 2024 - Till Date